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First Named Inventor	Blaise B. Fanning
Art Unit	2188
Examiner Name	Lane, John A.
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ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
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  - ☐ After Final
  - ☐ Affidavits/declaration(s)
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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Signature	
Date	November 3, 2004

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Signature		Date	**November 3, 2004**

AF IW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Blaise B. Fanning

Application No.: 09/751,602

Filed: December 29, 2000

Attorney Docket No.: 42390.P10585

For: METHOD AND APPARATUS FOR OPTIMIZING DATA STREAMING IN A COMPUTER SYSTEM UTILIZING RANDOM ACCESS MEMORY IN A SYSTEM LOGIC DEVICE

Examiner: Lane, John A.

Art Unit: 2188

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RESPONSE AFTER FINAL

In response to the final Office Action mailed September 3, 2004, Applicant respectfully requests that the following remarks be considered:

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Esther Campbell
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(Signature of person mailing correspondence)

IN THE CLAIMS

Claims 1, 2, 4-7, 10-12, 14-19, 22-23, and 27-33 are pending. No claims have been amended. A complete list of claims is presented below for the convenience of the Examiner:

1. (Previously presented) An apparatus comprising:

a processor interface unit; and

a cache to store information received from a processor coupled to the processor interface unit, the cache to store disposable information that may be overwritten without ever having delivered the disposable information to a system memory if the disposable information has been read at least once, the cache further including a cache management unit to determine whether a cache entry contains disposable information by comparing a disposable information cache entry address with a range of addresses that define a disposable information address space.

2. (Original) The apparatus of claim 1, the cache to further store non-disposable information.

3. Cancelled.

4. (Previously presented) The apparatus of claim 2, further comprising a bus interface unit to allow a device coupled to the bus interface unit to access the cache.

5. (Previously presented) The apparatus of claim 4, the cache management unit to allow the cache entry to be overwritten once the device coupled to the bus interface unit reads the cache entry and if the cache management logic determines that the cache entry contains disposable information.

6. (Original) The apparatus of claim 5, further comprising a system memory controller.

7. (Original) The apparatus of claim 6, the cache management unit to cause the cache entry contents to be delivered to the system memory controller for delivery to a system memory if the cache management unit determines that the cache entry does not contain disposable information.

8. Cancelled.

9. Cancelled.

10. (Previously presented) The apparatus of claim 7, further comprising at least one programmable register to store addresses that define a disposable address space.

11. (Previously presented) A system, comprising:

a processor; and

a system logic device coupled to the processor, the system logic device including

a processor interface unit, and

a cache to store information received from a processor coupled to the processor interface unit, the cache to store disposable information that may be overwritten without ever having delivered the disposable information to a system memory if the disposable information has been read at least once, the cache further including a cache management unit to determine whether a cache entry contains disposable information by comparing a disposable information cache entry address with a range of addresses that define a disposable information address space.

12. (Original) The system of claim 11, the cache to further store non-disposable information.

13. Cancelled.

14. (Previously presented) The system of claim 12, the system logic device further including a bus interface unit.

15. (Original) The system of claim 14, further comprising a device coupled to the system logic device bus interface unit.

16. (Previously presented) The system of claim 15, the cache management unit to allow the cache entry to be overwritten once the device coupled to the bus interface unit

reads the cache entry and if the cache management logic determines that the cache entry contains disposable information.

17. (Original) The system of claim 16, the system logic device further including a system memory controller.

18. (Original) The system of claim 17, further comprising a system memory coupled to the system memory controller.

19. (Original) The system of claim 18, the cache management unit to cause the cache entry contents to be delivered to the system memory controller for delivery to the system memory if the cache management unit determines that the cache entry does not contain disposable information.

20. Cancelled.

21. Cancelled.

22. (Original) The system of claim 21, the system logic device further including at least one programmable register to store addresses that define a disposable address space.

23. (Previously presented) A method, comprising:

receiving a line of information from a processor;

storing the line of information in a cache;

determining whether the line of information is disposable by comparing the address of the line of information with a range of addresses that defines a disposable information address space; and

overwriting the line of information, if it is determined to be disposable, without ever having written the line of information to a system memory once the line of information has been read by a system device.

24. Cancelled

25. Cancelled.

26. Cancelled.

27. (Previously presented) An apparatus comprising:

a processor interface unit; and

a cache to store information received from a processor coupled to the processor interface unit, the cache to store disposable information that may be overwritten without ever having delivered the disposable information to a system memory if the disposable information has been read at least once, the processor interface unit to receive a disposable information attribute indication from the processor when the processor delivers the disposable information to the processor interface unit.

28. (Previously presented) The apparatus of claim 27, the cache to further store non-disposable information.

29. (Previously presented) The apparatus of claim 28, further comprising a bus interface unit to allow a device coupled to the bus interface unit to access the cache.

30. (Previously presented) The apparatus of claim 29, the cache management unit to allow the cache entry to be overwritten once the device coupled to the bus interface unit reads the cache entry and if the cache management logic determines that the cache entry contains disposable information.

31. (Previously presented) The apparatus of claim 30, further comprising a system memory controller.

32. (Previously presented) The apparatus of claim 31, the cache management unit to cause the cache entry contents to be delivered to the system memory controller for delivery to a system memory if the cache management unit determines that the cache entry does not contain disposable information.

33. (Previously presented) A method, comprising:

receiving a line of information from a processor;

storing the line of information in a cache;

determining whether the line of information is disposable by examining an attribute communicated along with the line of information by the processor; and

overwriting the line of information, if it is determined to be disposable, without ever having written the line of information to a system memory once the line of information has been read by a system device.

REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1, 2, 4-7, 10-12, 14-19, 22-23, and 27-33 are pending. No claims have been canceled. No claims have been added. No claims have been amended.

Claims 1, 2, 4-7, 10-12, 14-19, 22, 23 and 27-33 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,414,644 of Tayler ("Tayler"). Applicant respectfully traverses the rejection.

Claim 1 sets forth a cache management unit to determine whether a cache entry contains disposable information by comparing a disposable information cache entry address with a range of addresses that define a disposable information address space. In contrast Tayler fails to disclose at least the above limitation.

The Examiner asserted that the cache management unit corresponds to the circuitry included within the storage director 11 in Tayler. The Examiner further asserted that "comparing a disposable information cache entry address with a range of addresses that define a disposable information address space" corresponds to accessing logical device control block (LDCB) 31 for identification (i.e., addresses) of data blocks to be deleted (i.e., marked as disposable). (Final Office Action, p. 3, ln. 4-12).

However, Tayler merely discloses:

> Since RAD 37 is set to the active condition and data block B has been altered by a previous sequence of operations (not shown), then buffer control 18 supplies a signal over line 44 to logic AND circuits 45 to transfer the identification of data block B to discard list 31 for the addressed logical device.
> (Tayler, col. 5, ln. 33-38).

Contrary to the Examiner's assertion, Tayler merely discloses transferring the identification of data block B (the data block to be discarded) to the discard list 31 for the

addressed logical device. According to Tayler, the list of data blocks to be discarded is passed from the discard list 31 at the end of a command chain (Tayler, col. 5, ln. 52-57). In other words, Tayler merely discloses transferring the identification of the data block to be discarded to the discard list 31 and then passing the list from the discard list 31. Tayler does not disclose, suggest, or imply ***comparing*** a disposable information cache entry address with a range of addresses that define a disposable information address space.

Furthermore, the Examiner argued that the claimed "range of addresses that defines a disposable information address space" corresponds to the fixed number of addressable storage registers. (Final Office Action, p. 3, ln. 12-16). However, the fixed number of addressable storage registers of the data blocks A-H in Tayler corresponds to different *logical devices* (Tayler, col. 3, ln. 27-35). The addressable storage registers of the data blocks in Tayler do not define a *disposable information address space.*

For at least these reasons, Tayler fails to anticipate claim 1. Withdrawal of the rejection is respectfully requested.

For at least the reasons discussed above with respect to claim 1, Tayler fails to anticipate claims 11, 23, 27, and 33. Withdrawal of the rejection is respectfully requested.

Claims 2, 4-6, 10, 12, 14-19, 22, and 28-32 depend, directly or indirectly, from claims 1, 11, 23, and 27. Therefore, Tayler fails to anticipate claims 2, 4-6, 10, 12, 14-19, 22, and 28-32 for at least the reasons discussed above with respect to claim 1. Withdrawal of the rejection is respectfully requested.

Applicant respectfully submits that the rejections have been overcome by the remarks, and that the pending claims are in condition for allowance. Accordingly,

Applicant respectfully requests the rejections be withdrawn and the pending claims be allowed.

If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: November 3, 2004

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